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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of

SANTHANA KRISHNAMACHARI

Atty. Docket

PHA 23,543A

Serial No.: 09/197,314

Group Art Unit: 2613

Filed: NOVEMBER 20, 1998

Examiner: R. LEE

Title: SYSTEM FOR PERFORMING RESOLUTION UPSCALING ON FRAMES OF DIGITAL VIDEO

Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed is an original plus two copies of an Appeal Brief in the above-identified patent application.

Please charge the fee of $320.00 to Deposit Account No. 14-1270.

Respectfully submitted,

By Russell Gross
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited this date with the United States Postal Service as first-class mail in an envelope addressed to:

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Washington, D.C. 20231

On February 3, 2003

By Edna Chagra

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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2-10-03

In re Application of Atty. Docket

SANTHANA KRISHNAMACHARI PHA 23,543A

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APPEAL BRIEF

Sir:

The rejection of Claims 1-7, 9-20, 22-33, 35-40 and 42-47 is hereby being appealed, which are produced in the attached Appendix.

1. Relay Party in Interest

The real party in interest is Philips Electronic North American Corporation, the assignee herein.

2. Related Appeals and Interferences

The Appellant is not aware of any appeals or interferences that relate to the present application.

3. Status of all Claims

Claims are currently pending in the present application. Claims 1-7, 9-20, 22-33, 35-40 and 42-47 were submitted in the present application when originally field. In the Office Action dated September 18, 2002, these claims were finally rejected.

4. Status of Amendment

No Amendments were filed subsequent to the Final Rejection of September 18, 2002.

5. Summary of the Invention

The present invention is directed to a method and apparatus for increasing a resolution of at least a portion of a reference frame of video. As can be seen from Figure 6, the present invention includes a first block of pixels being selected in the reference frame, as described on page 13 of the present application.

As described on pages 13-14, locating, in N (N≥1) target frames, one or more blocks of pixels that substantially correspond to the first block of pixels, where the N target frames are separate from the

reference frame. Further, determining values of additional pixels based on values of pixels in the first block and on values of pixels in the one or more blocks and adding the additional pixels among the pixels in the first block, as described on page 14.

6. Issues Presented for Review

The first issue is whether Claims 1-6, 8-19, 22-26, 40 and 45-46 under 35 USC 102 are anticipated by Ueno et al. (U.S. Patent No. 5,418,570). The second issue is whether Claims 42-43 under 35 USC 102 are anticipated by Yonemitsu et al. (U.S. Patent No. 5,475,435). The third issue is whether Claims 7 and 20 under 35 USC 103 are unpatentable over Ueno et al. in view of Guetz et al. (U.S. Patent No. 6,091,77). The fourth issue is whether Claims 27-32, 34-39 and 47 under 35 USC 103 is unpatentable over Ueno et al. in view of Lempel (U.S. Patent No. 6,115,070). The fifth issue is whether Claim 33 under 35 USC 103 is unpatentable over Ueno et al. in view of Lempel, and in further view of Guetz et al. The sixth issue is whether Claim 44 under 35 USC 103 is unpatentable over

Yonemitsu et al. in view of Song et al. (U.S. Patent No. 6,115,070).

7. Grouping of the Claims

The Appellant respectfully submits that the claims either stand or fall together.

8. Arguments

Claims 1-6, 8-19, 22-26, 40 and 45-46 stand rejected under 35 USC 102 as being anticipated by Ueno et al. (U.S. Patent No. 5,418,570). Claims 7 and 20 stand rejected under 35 USC 103 as being unpatentable over Ueno et al. in view of Guetz et al. (U.S. Patent No. 6,091,77). Claims 27-32, 34-39 and 47 stand rejected under 35 USC 103 as being unpatentable over Ueno et al. in view of Lempel (U.S. Patent No. 6,115,070). Claim 33 stands rejected under 35 USC 103 as being unpatentable over Ueno et al. in view of Lempel, and in further view of Guetz et al.

In order to make a proper anticipation rejection under 35 USC 102, Section 706.02 of the MPEP requires that a reference must teach every aspect of the claimed invention either explicitly or impliedly.

Further, in order to establish anticipation, it is incumbent upon the Examiner to identify in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. *Lindemann Mascinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458, (Fed. Cir. 1984).

In view of the above, it is respectfully submitted that the burden of showing that Ueno et al. anticipates all of the features recited in the claims has not been met. In particular, such features include "determining values of additional pixels based on values of pixels in the first block and on values of pixels in the one or more blocks", as recited in claims 1, 14, 27 and 40.

Initially, in addressing this feature in the above rejections, the upsampling circuit 35 shown in Figure 7 of Ueno et al. is being relied on. It was further stated by the Examiner that the low resolution local decoded signal 34 output from the local decoder 33 as shown in Figure 7 of Ueno et al. is actually based on first blocks of pixels in the reference frame and one or more blocks of pixels that substantially correspond

to the first block of pixels as provided by the search range calculation within coding section 30 of Figure 7 of Ueno et al. (See column 14, lines 33-41, column 16, lines 8-20).

In response, the Appellant has carefully reviewed the above portions and does not see where it supports the above interpretation of Ueno et al. In fact, these portions of Ueno et al. do not even mention the upsampling circuit 35, local decoder 33 and coding section 30 of Figure 7, as mentioned above.

Moreover, in column 19, lines 41-54, Ueno et al. discloses a signal obtained by horizontal upsampling...is separated into an odd-field signal and even-field signal in a first filed separator 402. Ueno et al. further discloses that the odd-field signal and even-field signal are subjected to vertical interpolation.

Based on the above disclosure, it is evident that the up-sampling of Ueno et al. does not perform "determining values of additional pixels based on values of pixels in the first block and on values of pixels in the one or more blocks", as required by the claims. However, despite this point, the above

rejections were maintained in the Final Office Action of September 18, 2002.

In maintaining these rejections, it was stated that the presently recited "determining values of additional pixels based on values of pixels in the first block and on values of pixels in the one or more blocks" is disclosed in column 8, line 41 to column 9, line 34, column 12, line 35 to column 13, line 60, column 15, lines 33-41, and column 16, lines 8-20, of Ueno et al. However, after carefully reviewing these portions of Ueno et al., the Appellant still does not see where such a feature is disclosed.

Further, in maintaining these rejections, the Examiner appears to be relying on the vertical interpolation disclosed in column 19, lines 41-54, of Ueno et al. However, in this portion, Ueno et al. only discloses that an odd field signal and even field signal are subjected to a vertical interpolation. Based on this disclosure, it is evident that individual fields are only being interpolated. Thus, it is unreasonable to interpret this as "determining values of additional pixels based on values of pixels in the first block and on values of pixels in the one

or more blocks", as required by the claims. Therefore, it is respectfully submitted that this feature is not anticipated by Ueno et al.

The above-described deficiencies of Ueno et al. are also not addressed by either Lempel or Guetz et al. since they are being relied on for other features. Thus, the invention of Claims 1-7, 9-20, 22-33, 35-40 and 45-47 is neither anticipated nor made obvious by Ueno et al. alone or in combination with either Lempel or Guetz et al. Therefore, the Appellant respectfully requested that these rejections be reconsidered and reveresed.

Claims 42-43 stand rejected under 35 USC 102 as being anticipated by Yonemitsu et al. (U.S. Patent No. 5,475,435). Claim 44 stands rejected under 35 USC 103 as being unpatentable over Yonemitsu et al. in view of Song et al. (U.S. Patent No. 6,115,070).

In response, it is also respectfully submitted that the burden of showing that Yonemitsu et al. anticipates all of the features recited in the claims has not been met. In particular such features include "a processor which increases a resolution of a reference frame of the video based on pixels in the

reference frame and based on pixels in at least one other target frame of the video", as recited in claim 42.

In initially addressing this feature in the above rejections, the up sampling circuit 57 of Yonemitsu et al. is being relied on. However, in column 7, lines 11-13, Yanemitsu et al. discloses that the lower layer is input to the up sampling circuit 57, in which it is processed by interpolation so that its converted into a non-interlace picture.

Based on the above disclosure, it is evident that the up sampling circuit 57 of Yonemitsu et al. does not "increase a resolution of a reference frame of the video based on pixels in the reference frame and based on pixels in at least one other target frame of the video", as required by the claims. However, despite this point the above rejections were maintained in the Final Office Action of September 18, 2002.

In maintaining these rejections, it was stated that the interpolation process provided within the upsampling circuit 57 of Yanemitsu et al. provides the same increase in resolution of a reference frame of

the video based on pixels in the reference frame and at least one other target frame.

However, in column 7, lines 11-13, Yonemitsu et al. clearly discloses that the output picture S66 of the lower layer is input to the up sampling circuit 57, in which it is processed by interpolation so that its converted into a non-interlace picture. Based on this disclosure, it is evident that only a single picture is interpolated. Thus, it is evident that the up sampling circuit 57 of Yonemitsu et al. does not "increase a resolution of a reference frame of the video based on pixels in the reference frame and based on pixels in at least one other target frame of the video", as required by the claims. Therefore, it is respectfully submitted that this feature is not anticipated by Yonemitsu et al.

The above-described deficiencies of Yonemitsu et al. are also not addressed by Song et al. Thus, the invention of claims 42-44 is neither anticipated nor made Yonemitsu et al. alone or in combination with Song et al. Therefore, the Appellant respectfully requests that these rejections also be reconsidered and reversed.

Please charge the fee of $320.00 to Deposit Account No. 14-1270.

Respectfully submitted,

By _____
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CERTIFICATE OF MAILING

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COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

On February 3, 2003

By Edna Chagra

A P P E N D I X

1. A method of increasing a resolution of at least a portion of a reference frame of video, the method comprising the steps of:

selecting a first block of pixels in the reference frame;

locating, in N (N≥1) target frames, one or more blocks of pixels that substantially correspond to the first block of pixels, where the N target frames are separate from the reference frame;

determining values of additional pixels based on values of pixels in the first block and on values of pixels in the one or more blocks; and

adding the additional pixels among the pixels in the first block.

2. A method according to Claim 1, wherein the N target frames comprise frames of video which were predicted, at least in part, based on pixels in the reference frame.

3. A method according to Claim 1, wherein the determining step determines the values of the additional pixels based also on coefficients which are weighted in accordance with the first block and the one or more blocks.

4. A method according to Claim 3, wherein the coefficients are weighted based on differences between pixels in the first block and pixels in each of the one or more blocks.

5. A method according to Claim 4, wherein the differences comprise a residual.

6. A method according to Claim 1, wherein, in a case that the locating step does not locate any blocks of pixels in the target frames that substantially correspond to the first block of pixels, the determining step determines the values of the additional pixels based on values of pixels in the first block without regard to values of pixels in the N target frames (S606).

7. A method according to Claim 6, wherein the determining step determines the values of the additional pixels by performing bilinear interpolation using at least some of the pixels in the first block.

9. A method according to claim 1, wherein the reference frame comprises a bi-directional (B) frame; and

wherein the method further comprises, before the selecting step, the step of determining a location of the first block in the reference frame based on blocks of pixels in frames which precede and which follow the reference frame.

10. A method according to claim 1, wherein the reference frame comprises one of an intramode (I) frame and a predictive (P) frame; and

wherein the N target frames comprise at least one of a P frame and a bi-directional (B) frame.

11. A method according to Claim 1, further comprising the step of changing distances between pixels in the first block in order to change a size of the first block.

12. A method according to Claim 1, wherein the locating step uses motion vectors from the reference frame to the target frame to locate the one or more blocks of pixels.

13. A method according to Claim 1, wherein the locating step searches through the N target frames to locate the one or more blocks of pixels.

14. Computer-executable process steps stored on a computer-readable medium, the computer-executable process steps to increase a resolution of at least a portion of a reference frame of video, the computer-executable process steps comprising:

code to select a first block of pixels in the reference frame;

code to locate, in N ($N \geq 1$) target frames, one or more blocks of pixels that substantially correspond to the first block of pixels, where the N target frames are separate from the reference frame;

code to determine values of additional pixels based on values of pixels in the first block and on values of pixels in the one or more blocks; and

code to add the additional pixels among the pixels in the first block.

15. Computer-executable process steps according to Claim 14, wherein the N target frames comprise frames

of video which were predicted, at least in part, based on pixels in the reference frame.

16. Computer-executable process steps according to Claim 14, wherein the determining code determines the values of the additional pixels based also on coefficients which are weighted in accordance with the first block and the one or more blocks.

17. Computer-executable process steps according to Claim 16, wherein the coefficients are weighted based on differences between pixels in the first block and pixels in each of the one or more blocks.

18. A method according to Claim 17, wherein the differences comprise a residual.

19. Computer-executable process steps according to Claim 14, wherein, in a case that the locating code does not locate any blocks of pixels in the target frames that substantially correspond to the first block of pixels, the determining code determines the values of the additional pixels based on values of pixels in the first block without regard to values of pixels in the N target frames.

20. Computer-executable process steps according to Claim 19, wherein the determining code determines the values of the additional pixels by performing bilinear interpolation using at least some of the pixels in the first block.

22. Computer-executable process steps according to claim 14, wherein the reference frame comprises a bi-directional (B) frame; and

wherein the computer-executable process steps further comprise a code to determine a location of the first block in the reference frame based on blocks of pixels in frames which precede and which follow the reference frame.

23. Computer-executable process steps according to claim 14, wherein the reference frame comprises one of an intramode (I) frame and a predictive (P) frame; and

wherein the N target frames comprise at least one of a P frame and a bi-directional (B) frame.

24. Computer-executable process steps according to Claim 14, further comprising code to change distances between pixels in the first block in order to change a size of the first block.

25. Computer-executable process steps according to Claim 14, wherein the locating code uses motion vectors from the reference frame to the target frame to locate the one or more blocks of pixels.

26. Computer-executable process steps according to Claim 14, wherein the locating code searches through the N target frames to locate the one or more blocks of pixels.

27. An apparatus for increasing a resolution of at least a portion of a reference frame of video, the apparatus comprising:

a memory which stores computer-executable process steps; and

a processor which executes the process steps so as (i) to select a first block of pixels in the reference frame, (ii) to locate, in N ($N \geq 1$) target frames, one or more blocks of pixels that substantially correspond to the first block of pixels, where the N target frames are separate from the reference frame, (iii) to determine values of additional pixels based on values of pixels in the first block and on values of pixels in the one or more blocks, and (iv) to add the additional pixels among the pixels in the first block.

28. An apparatus according to Claim 27, wherein the N target frames comprise frames of video which were predicted, at least in part, based on pixels in the reference frame.

29. An apparatus according to Claim 27, wherein the processor determines the values of the additional pixels based also on coefficients which are weighted in accordance with the first block and the one or more blocks.

30. An apparatus according to Claim 29, wherein the coefficients are weighted based on differences between pixels in the first block and pixels in each of the one or more blocks.

31. An apparatus according to claim 30, wherein the differences comprise a residual.

32. An apparatus according to Claim 27, wherein, in a case that the processor does not locate any blocks of pixels in the target frames that substantially correspond to the first block of pixels, the processor determines the values of the additional pixels based

on values of pixels in the first block without regard to values of pixels in the N target frames.

33. An apparatus according to Claim 32, wherein the processor determines the values of the additional pixels by performing bilinear interpolation using at least some of the pixels in the first block.

35. An apparatus according to claim 27, wherein the reference frame comprises a bi-directional (B) frame; and

wherein, before selecting the first block, the processor executes process steps so as to determine a location of the first block in the reference frame based on blocks of pixels in frames which precede and which follow the reference frame.

36. An apparatus according to claim 27, wherein the reference frame comprises one of an intramode (I) frame and a predictive (P) frame; and

wherein the N target frames comprise at least one of a P frame and a bi-directional (B) frame.

37. An apparatus according to Claim 27, wherein the processor executes process steps so as to change distances between pixels in the first block in order to change a size of the first block.

38. An apparatus according to claim 27, wherein the processor uses motion vectors from the reference frame

to the target frame to locate the one or more blocks of pixels.

39. An apparatus according to claim 27, wherein the processor searches through N target frames to locate the one or more blocks of pixels.

40. An apparatus for increasing a resolution of at least a portion of a reference frame of video, the apparatus comprising:

means for selecting a first block of pixels in the reference frame;

means for locating, in N ($N \geq 1$) target frames, one or more blocks of pixels that substantially correspond to the first block of pixels, where the N target frames are separate from the reference frame;

means for determining values of additional pixels based on values of pixels in the first block and on values of pixels in the one or more blocks; and

means for adding the additional pixels among the pixels in the first block.

42. A television system which receives coded video data, and which forms images based on the coded video data, the television system comprising:

a decoder which decodes the video data to produce frames of video;

a processor which increases a resolution of a reference frame of the video based on pixels in the reference frame and based on pixels in at least one other target frame of the video; and

a display which displays an image based on the reference frame;

wherein the processor increases the resolution of the reference frame by selecting blocks of pixels in the reference frame and, for each selected block, (i) locating, in N (N≥1) target frames, one or more blocks of pixels that substantially correspond to the first block of pixels, where the N target frames are separate from the reference frame; (ii) determining values of additional pixels based on values of pixels in the selected block and on values of pixels in the one or more blocks, and (iii) adding the additional pixels among the pixels in the selected block.

43. A television system according to Claim 42, wherein, in a case that the processor does not locate any blocks of pixels in the target frames that substantially correspond to the selected block of pixels, the processor determines the values of the additional pixels based on values of pixels in the

selected block without regard to values of pixels in the N target frames.

44. A television system according to Claim 42, wherein the decoder and the processor are implemented in a settop box.

45. A method according to Claim 4, wherein the locating step locates the one or more blocks using motion vectors present in a coded bitstream for the target frames; and

wherein the coefficients are determined using DCT values of at least one coded residual, where the at least one coded residual comprises differences between the reference frame and the target frame(s).

46. Computer-executable process steps according to Claim 17, wherein the locating code locates the one or more blocks using motion vectors present in a coded bitstream for the target frames; and

wherein the coefficients are determined using DCT values of at least one coded residual, where the at least one coded residual comprises differences between the reference frame and the target frame(s).

47. An apparatus according to Claim 30, wherein, in a case that the reference and target frames of video are coded using MPEG, the locating step locates the one or

more blocks using motion vectors present in an MPEG bitstream for the target frames; and

wherein the coefficients are determined using DCT values of at least one coded residual, where the at least one coded residual comprises differences between the reference frame and the target frame(s).